DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 42, 43 and 49 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 42 and 49 recite "at least one electrostatic discharge device disposed between one said bond pad and extending at least partially beneath said bond pad;". It is unclear exactly what the electrostatic discharge device is disposed between; the device cannot be disposed between a single given location (one bond pad), there must be two locations for a device to be between them.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Insofar as definite, claims 42, 43 and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tamura '068 in view of Countryman et al. '892.

Tamura discloses a semiconductor wafer comprising a plurality of integrated circuits (figs 1A & 2A; col. 1, lines 39-40; integrated circuit separated from wafer, which inherently has a plurality of circuits before separation) and a method of manufacturing

thereof, wherein each of the integrated circuits is separated from the other of the integrated circuits by a scribe region (fig. 2, chip edge 204 is where dicing occurred, thus the scribe region) at the periphery of each the integrated circuit; providing a centrally disposed core region (figs. 2 & 4, "core logic") in each of the circuits; providing at least one bond pad (fig. 2, 208A) disposed between the core region and the scribe region; providing at least one electrostatic discharge device (210a); and providing an I/O buffer (fig. 2, I/O cell 225a; col. 1, lines 50-53, I/O cells contain I/O buffers) extending unimpeded (fig. 2, I/O buffer extends electrically unimpeded from the scribe region to the core circuitry by the shown wiring interconnects) from the scribe region to the core region and disposed laterally of the bond pad relative to the core region and the scribe region.

Tamura does not explicitly disclose the electrostatic discharge device to be disposed at least partially beneath the bond pad. Countryman teaches an integrated circuit device and method of manufacturing thereof comprising the steps of: providing a semiconductor substrate (fig. 5, 32) which includes a scribe (fig. 4, chip separation boundaries are shown by metallization 20, which is inherently the scribe region) at the periphery of the substrate and a centrally disposed core region (fig. 1; col. 2, lines 35-40, circuit 10 has devices within it, considered core circuits); providing at least one bond pad (fig. 5, 20) disposed between the core region and the scribe region (fig. 1); providing a electrostatic discharge device (fig. 5, diodes 26/40, 27/41, etc) disposed at least partially beneath the bond pad; and providing an I/O buffer disposed between the scribe region and the core region (fig. 1, 22/24; col. 2, lines 35-40).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to disposed the electrostatic discharge device of Tamura at least partially beneath the bond pad as taught by Countryman. One would have been motivated to do this because Countryman taught that disposing the electrostatic discharge device at least partially beneath the bond pad reduces the required area for the ESD device (Countryman; col. 2, lines 4-19), thus allowing the chips to be made smaller as desired by chip designers and manufacturers (col. 2, lines 21-31). The teaching of Countryman is especially applicable to figure 4 of Tamura, where Tamura shows the EDS devices 210 occupying extra space between the chip edge and the core logic area, wherein this space would be reduced if ESD device 210 was partially formed under bond pad 208 of fig. 2.

Response to Arguments

5. Applicant's arguments with respect to claims 42, 43 and 49 have been fully considered but they are not persuasive. Applicant argues that Tamura does not teach the I/O buffer to extend unimpeded from the scribe region to the core region. This argument is not persuasive because Tamura teaches the I/O buffer to extend electrically unimpeded from the scribe region to the core circuitry by the shown wiring interconnects (fig. 2). The claims are written broadly enough to be anticipated by this disclosure.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to STEVEN J. FULK whose telephone number is (571)272-8323. The examiner can normally be reached on Monday through Friday, 8:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on (571) 272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

8. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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/Douglas M Menz/
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